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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,872	06/28/2001	Tatsuya Shimoda	109975	3054

25944 7590 06/10/2002

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EXAMINER

BAUMEISTER, BRADLEY W

ART UNIT PAPER NUMBER

2815

DATE MAILED: 06/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

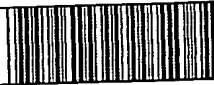
Office Action Summary

Application No.
09/892,872

Applicant(s)
Shimoda et al.

Examiner
B. William Baumeister

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2815



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on May 15, 2002
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above, claim(s) 7, 11, and 17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-10, 12-16, and 18-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on Jun 28, 2001 is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 3

4) ☐ Interview Summary (PTO-413) Paper No(s). _____

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other:

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DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restriction

2. Applicant's election with traverse of I in Paper No. 14 is acknowledged. The traversal is on the ground(s) that the subject matter of the various inventions is so sufficiently related that a thorough search would not constitute an undue burden. This is found to be partially persuasive. Upon further consideration, the Examiner is of the opinion that it would not constitute an undue burden to rejoin and additionally examine the claims of inventions II-IV with the claims of elected invention of Group I. However, Applicant has alleged no errors in the restriction requirement, and the Examiner is still of the opinion that it would constitute an undue burden to examine claims directed towards either of inventions V or VI for the reasons set forth therein. Accordingly:

- a. Inventions I-IV are rejoined; claims 1-6, 8-10, 12-16 and 18-25 are rejoined/under active consideration.

- b. Claims 7 & 17 and claim 11 remain withdrawn for being directed towards non-elected inventions V and VI, respectively.

The requirement is still deemed proper and is therefore made FINAL.

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Drawings

3. Figure 24-26A/C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-6, 8-10, 12-16 and 18-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. '186 (supplied in IDS, paper #3) in view of Applicant's Prior Art Admissions.

a. Smith discloses shaped microstructures that are assembled into appropriately-shaped binding-site receptor recesses formed in a substrate through fluid transport (e.g., ABSTRACT). Smith teaches that the microstructures may support a wide range of devices such as diodes, transistors, integrated circuits, display devices, etc. (e.g., col. 1, lines 30-34). Smith further teaches that the microstructures are not limited to GaAs, but may also comprise, *inter*

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alia, other material systems such as Si, other group-IV, III-V or II-VI material systems (col. 4, lines 55). Also, the substrate on which the microstructures are assembled may be composed of Si or GaAs wafers, plastic sheets (e.g., a photocurable resin), glass or ceramic substrates, or “almost any type of material capable of forming recessed regions or generally binding sites or receptors thereon which complement the shaped blocks.” (Col. 14, lines 18-24 and col. 13, lines 60-62 which specifically recites molded plastic sheets). Further, Smith teaches that applications which require a number of different larger circuits could be realized by etching the microstructures into specific shapes and assembling them into matching recessed regions (col. 11, lines 38-44). Smith does not teach that ferroelectric-capacitor passive matrix arrays and/or associated peripheral circuits, specifically, may be employed within the Smith microstructure-on-substrate invention.

b. Applicant admits that ferroelectric capacitor passive matrix arrays (ferroelectric PMAs) operated by peripheral circuits are known, and that both can be grown on Si substrates. (See the BACKGROUND OF THE INVENTION section of the specification.) Applicant also acknowledges that the manufacture of integrated FEPMA's with peripheral-circuit MOS transistors was known and that it was known that this integration poses the drawback of less than optimal device performance (paragraphs [0009]-[0011]).

c. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have grown the conventional FEPMA's and peripheral circuits separately and integrate them onto a common substrate through the microstructure techniques taught by Smith for the purpose of obviating the device performance drawbacks which applicant acknowledges

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were known. Further, it would have been obvious to one of ordinary skill in the art at the time of the invention that either specific one of the FEPMA or the peripheral circuit could be formed on a microstructure or substrate, respectively, or that both could be formed on separate microstructures and respectively assembled to a substrate, and that undertaking any particular one of these options would not produce any unexpected results; but rather, the specific option chosen would merely be determined by conventional manufacturing considerations such as (1) the space and layout requirements for the respective options; (2) the amount of wirebonding respectively required; (3) the application for which the memory device is ultimately to be employed, which in turn, would dictate such considerations as what other devices/circuits are to be integrated on or connected to the substrate and/or microstructure(s), the amount of memory required (dictating how many FEPMA's are required) and whether an inexpensive or flexible plastic would be useful as a substrate.

d. With respect to claim 9, the Examiner notes that "a microstructure" reads on a Si chip. As such, the claim recitation--that the FEPMA and the peripheral circuit are integrated on a single microstructure--reads on Applicant's prior art FIGs 24-26A/C. Similarly, claims 10 and 18 read on a microstructure that is assembled on a Si substrate; and the language "a part of the second microstructure to be integrated" (e.g., claim 10, line 6) merely sets forth the intended use of a Si chip. As such, the claim is rendered obvious by a microstructure on a Si chip so long as the chip is *capable* of, in turn, being integrated onto some other substrate (e.g., a piece of plastic or a PCB).

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INFORMATION ON HOW TO CONTACT THE USPTO

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister**, at **(703) 306-9165**. The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

A handwritten signature in black ink, appearing to read 'B. William Baumeister', with a stylized, flowing script.

B. William Baumeister

Patent Examiner, Art Unit 2815

June 8, 2002